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# High-resolution phase-only spatial light modulators with sub-millisecond response

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## ABSTRACT

Improvements in silicon foundry processes have made possible high-resolution, light-efficient backplanes capable of driving electro-optic modulators with higher voltage signals. The higher voltage provides the excitation to achieve sub-millisecond response times with a wave of phase modulation when used with dual-frequency nematic liquid crystals. By combining dual-frequency phase modulators with high-voltage silicon backplanes, compact spatial light modulators become available for applications that need fast, high-throughput modulators such as optical signal processing, adaptive wavefront correction, optical signal routing or beamsteering, and active diffractive optics.

Keywords: Liquid crystal on silicon, dual-frequency, phase-only modulation, spatial light modulators

## 1. INTRODUCTION

Liquid crystal on silicon (LCoS) spatial light modulators (SLMs) using nematic and ferroelectric liquid crystal (FLC) modulators have existed for several years.<sup>1,2,3</sup> The ferroelectric and nematic liquid crystal (LC) materials allow the SLM to produce amplitude and phase modulation with different performance characteristics.<sup>4,5</sup> One of the most useful forms is phase-only modulation with at least one wave ( $0$  to  $2\pi$ ) of stroke. Phase-only modulation allows patterns to be encoded on the wavefront without attenuating the incident beam. Attenuation removes energy from the signal, adding heat to the modulator. Therefore, high efficiency is essential for light-starved or high-power systems. Normally, nematic LC is used for analog phase-only modulators, since these materials directly provide optical path differences (OPD) when the LC's birefringence is used to control the light's speed of propagation through the modulating layer. Unfortunately, the response time of these nematic modulators is strongly related to the addressing field used to control the OPD.

Response times in the tens of milliseconds are associated with high-resolution LCoS SLM's having a wave of stroke in the visible and near-IR. For these high-resolution LCoS SLMs, the addressing field is limited to a few volts by the backplane, which impedes the operating speed of the phase-only SLM. For many applications, sub-millisecond operating speeds are desired, which requires the backplane to provide more voltage at the pixel. Today, there are high-voltage foundry processes with sub-micron lithography. However, the transistor size grows as operating voltage increases, affecting pixel pitch. Large pixels are not desirable for compact correlator applications, since the optical path length of the system has to grow to compensate for the smaller angular spread in the spatial frequency components. In addition to application issues, fabrication of large arrays becomes a problem, if the pixel size is not restricted. The trade-off between higher voltage and smaller pixels creates a compromise, where the backplane voltage is still limited to 15 volts or less for pixel pitches of 25 microns or less. This voltage capability represents at most a factor of three improvement over existing high-resolution backplanes, which correlates to less than a factor of two improvement in speed (speed roughly increases with the square of the voltage) for normal nematic modulators. Therefore, sub-millisecond operation requires interfacing the higher voltage backplane with a different type of nematic material. This material has a frequency-dependent dielectric anisotropy, allowing faster response times.

Most commonly used nematic liquid crystals exhibit a positive dielectric anisotropy. This means that they can be rapidly driven from an optically thick state (more path delay) to an optically thin state. However, for conventional materials, going from an optically thin state to an optically thick state requires time for the molecules to relax. The relaxation time is a function of the cell's thickness, viscosity of the material and elastic forces that align the LC. Relaxation occurs faster when there is no electric field to counteract the alignment forces. It is the relaxation that is relatively slow.

Instead of relying on relaxation, it is possible to drive the molecules back to increase the optical path, if the dielectric anisotropy of the nematic LC changes sign. That is, the difference in the dielectric constants, which drives the LC transition, has a polarity change with the higher value at low frequencies dropping below the smaller value as the frequency of the drive signal increases. The sign change occurs at relatively low frequencies in certain types of materials. These materials are called dual-frequency nematics. Spatial light modulators with as many as 127 elements have been demonstrated using the dual-frequency effect.<sup>6</sup> In these devices, the pixel count is low enough that direct addressing is used, where there is a direct connection to each pixel in the array. A direct connection allows the voltage level and waveform of the drive signal to have considerable flexibility. With LCoS SLMs, its active-matrix addressing allows the modulator to have several thousands elements (e.g.  $256 \times 256 = 65,536$ ), but the active-matrix circuits place more restrictions on the drive signal.

An investigation of some of these materials indicates that sub-millisecond response times for a modulation depth of  $2\pi$  does not require an excessive amount of voltage ( $\pm 12$  volts peak-to-peak produces a 0.16 millisecond response as shown in Figure 1). However, this type of modulator requires an addressing technique that provides a high frequency excitation (about 40 kHz) to produce the sign-changing drive signal. By applying a high-frequency drive signal, the LC modulator is quickly reset to "relaxed" state, allowing data written to the SLM to be valid within a millisecond given that the VLSI backplane has sufficient voltage.

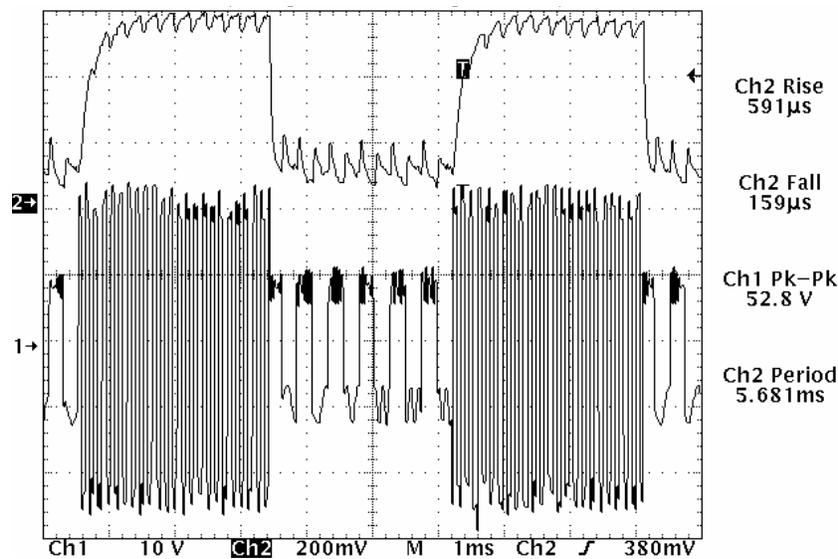


Figure 1: Oscilloscope outputs showing the drive signal (Ch1 - bottom trace) and the corresponding optical response (Ch2 - top trace) of a single-cell dual-frequency LC modulator. The on-to-off transition represents a  $\pi$  phase change for the transmissive cell, which is a  $2\pi$  phase change in reflection.

To drive the dual-frequency liquid crystal materials with a high-resolution backplane, higher voltage levels are required than the standard 3.3 - 5 volt capability available from most sub-micron semiconductor processes. There

are now 12 to 40 volt processes using sub-micron lithography. By using a moderate voltage (15 volts or less), it is possible to keep the pixel small and still provide sufficient voltage to drive the dual frequency modulator.

Recently, a high-voltage 256 x 256 LCoS SLM has been developed. The chip was fabricated through a 0.5- $\mu\text{m}$  foundry process that uses chemical-mechanical polishing (CMP) to eliminate surface variations due to underlying circuit structures. The device has a pixel pitch of 24- $\mu\text{m}$  with a flat fill factor of approximately 90%. The device provides 12 to 14 volts at the pixel. The load period for one frame of data is 115  $\mu\text{s}$ . This paper describes some of the initial results using this backplane with a dual-frequency modulator.

## 2. 256 x 256 HIGH-VOLTAGE BACKPLANE

Figure 2 shows a layout of the high-voltage (HV) 256x256 chip. The addressing circuitry is at the top of the chip. This circuit multiplexes 32 analog inputs into the 256 x 256 pixel array located in the active area. The active area is 6.144 mm (256 x 24  $\mu\text{m}$ ) per side. The circuit area to the left of the dummy pixel area contains test structures used to verify electrical performance of the chip.

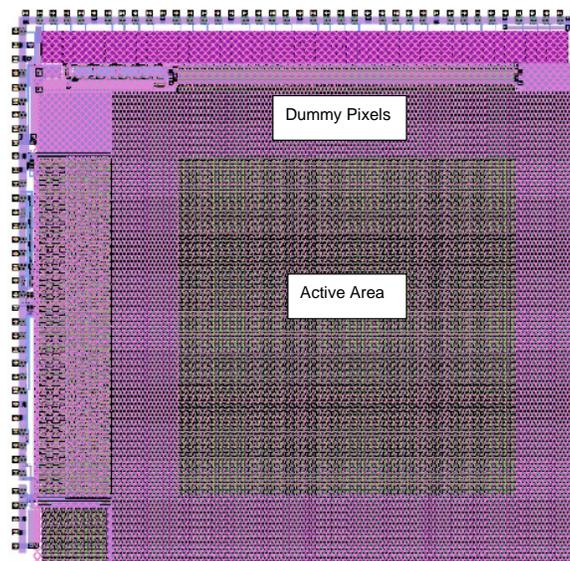


Figure 2. The HV 256x256 chip. The active area is only 36 % of the die size, due to the additional dummy pixels.

As shown above, the active area is surrounded by dummy pixels which reduce the adverse effects of chemical-mechanical polishing (CMP). CMP locally planarizes the die, removing the variations caused by the successive depositions and etching procedures used to fabricate the underlying circuitry. The planarization procedure provides tremendous improvement in the local flatness of the pixel. However, CMP is performed on the entire wafer. Between the individual die on the wafer are “scribe lines” to facilitate the cutting apart of the die on the wafer. These scribe lines produce local hills and valleys that affect the height of the polished layers. Subsequent layers conform and accentuate these irregularities. The dummy pixels provide a 1.2 mm buffer zone from these areas to spread the dome produced by the CMP process over a larger area. With most of the curvature being at the edge of the die (outside of the active area), this configuration produces a flatter active area.

The Zygo Interferometer scans shown in Figures 3 and 4 provide data on the curvature of the HV 256x256 die. Figure 3 represents the total pixel area including the dummy pixels. The size of this area is 9mm x 9mm. As shown in Figure 3, there are 0.8 waves of variation from center to edge. However, the active area represented by the plots in Figure 4 has considerably less curvature.

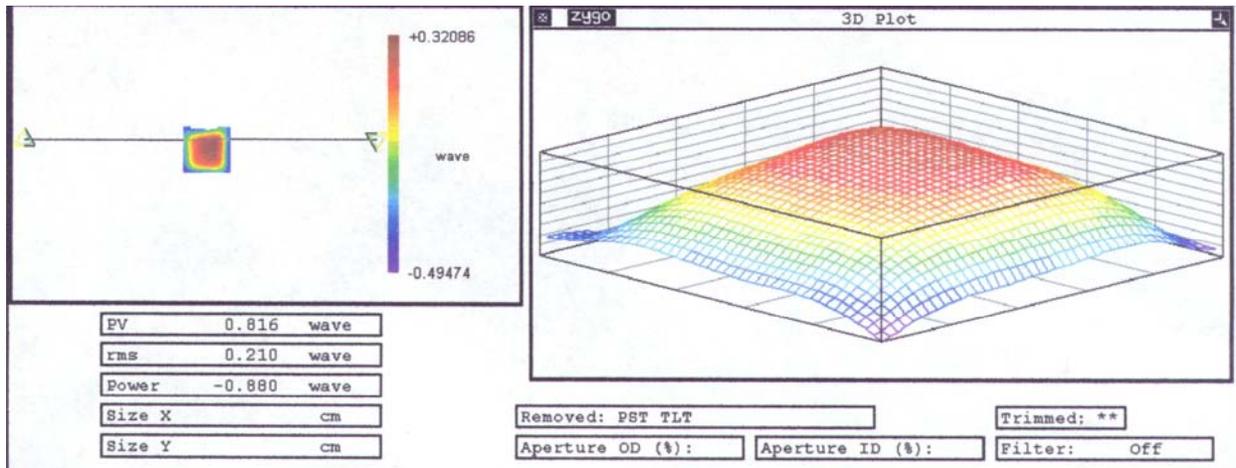


Figure 3. Zygo plot of the high-voltage backplane's pixel area including the dummy pixels surrounding the active area.

Figure 4 shows the curvature over the 6mm x 6mm active area of the die. Over this smaller area, the curvature is approximate a third of a wave with most of the active area being within a tenth of a wave. Nearly all of the curvature occurs at the very edge of the active area. These Zygo plots confirm that the dummy pixels act as a buffer zone, reducing the adverse effects of CMP processing.

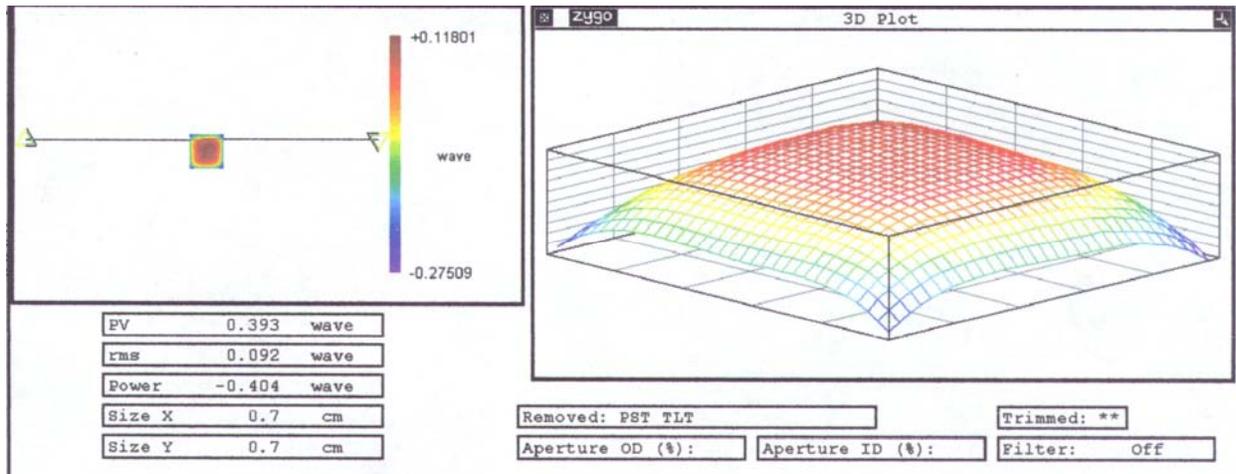


Figure 4. Zygo plot of high-voltage backplane's 256x256 active area.

The zero-order diffraction efficiency of the high-voltage 256x256 backplane was measured. As shown in Figure 5, a laser was used to illuminate the SLM backplane. The spot from the 532 nm laser was smaller than the active area of the die. A Newport power meter was used to measure the incident and reflected beams. An iris was used to isolate the zero-order component in the far field. This measurement accounts for all zero-order losses (diffraction and insertion). A metal mirror from the wafer, a raw backplane and a fully assembled SLM with a dual-frequency modulator was measured (refer to Table 1). These measurements allowed us to isolate some of the losses.

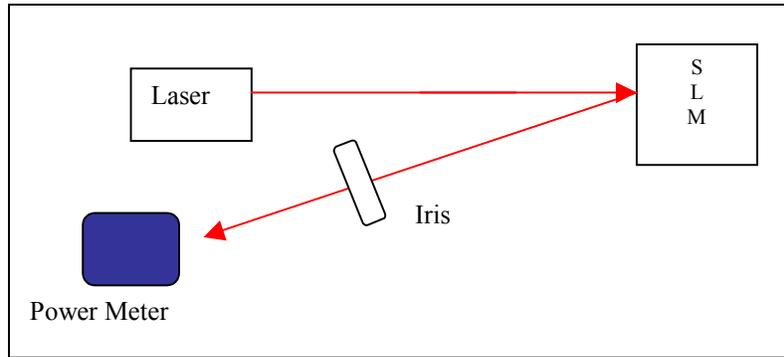


Figure 5. Optical setup for diffraction efficiency tests.

Device	Zero-Order Diffraction
Laser Power	100% (11.1 mW)
VLSI metal	88% (9.8mW)
Raw 256x256 Backplane	69% (7.65 mW)
Dual-frequency 256x256 SLM	63% (7.0 mW)

Table 1. Diffraction Efficiency Measurements

The raw backplane diffraction efficiency along with the metal reflectivity demonstrates that the actual pixel fill factor is approximately 89% (i.e. fill factor = square root [zero-order diffraction/metal reflectivity]). The pixel mirrors were designed to be 22.8 microns square on a 24-micron pitch, which provides a 90% fill factor. However, this fill factor does not include dimples due to vias. The last line in the table demonstrates that an assembled SLM has other significant insertion losses. These losses are from the coverglass, ITO electrode and liquid crystal. Most of the loss is due to Fresnel reflections at the different indexes. However, a small percentage is due to absorption and scatter from the ITO and liquid crystal.

### 3. DUAL-FREQUENCY LCOS SLM

The primary goal of this development was to achieve sub-millisecond  $2\pi$  phase modulation using a dual frequency modulator driven by a high-voltage 256 x 256 backplane. To achieve sub-millisecond response, several modulator configurations were investigated. Also, the operating temperature of the modulators was varied. The various changes made some difference in response, but the largest improvement came from optimizing the drive scheme. The proprietary drive scheme uses a combination of high and low frequency drive signals to quicken the modulator's response.

Figure 6 shows an oscilloscope trace where the waveform is from a high-speed detector that is receiving modulated light from the 256 x 256 SLM displaying monotone images (all pixels on or off). The SLM is operating between crossed polarizers with the optic axis of the SLM's modulator at  $45^\circ$  with respect to the polarizer's axes. This configuration converts a 0 to  $2\pi$  change in retardance to an off-to-on-to-off transition. In less than one millisecond, the modulator transitions from 0 to  $2\pi$  or  $2\pi$  to 0, depending on the drive voltage to the pixels (all pixels on - 12 volts / all pixels off - 0 volts).

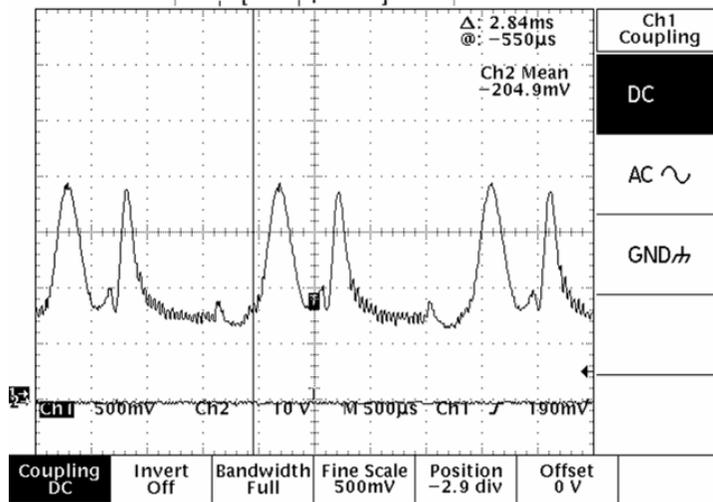


Figure 6. Off-to-on-to-off modulation representing  $2\pi$  of phase modulation at 670 nm in less than 1 millisecond.

The voltage level at the pixel controls the change in retardance that occurs during the data period. Figure 7 shows a scope trace from the high-speed detector as the SLM system runs a sequence of images. Each image is a different data level ranging from zero (left side of pattern) to 255 (right side of pattern). Each image is repeated several times to produce the stair steps. The spikes occurring in each stair step are from resetting the modulator during each image cycle. The spikes become larger as the retardance difference between the reset and data levels increase with the far left and far right sides of the pattern representing compressed versions of the transitions shown in Figure 6. Figure 8 is an image from the SLM operating at 1085 fps with the drive scheme.

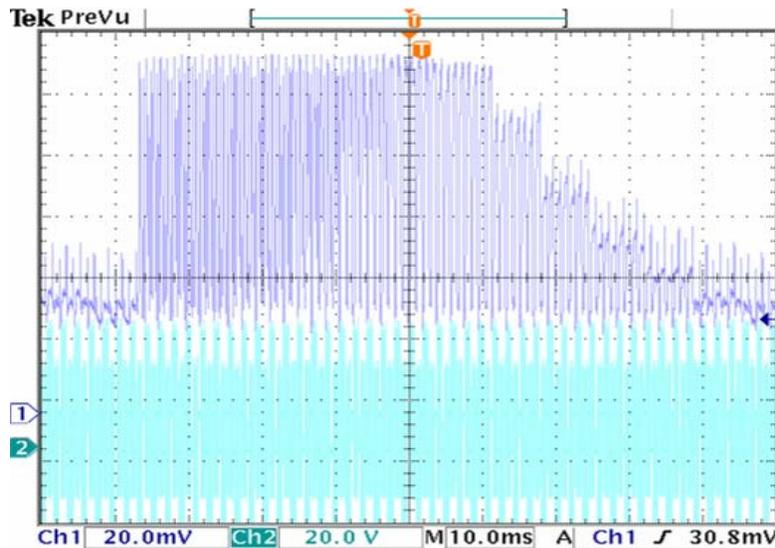


Figure 7. Scope trace showing the intensity levels generated by writing different data values to the SLM. Each sub-millisecond frame cycle includes a data and reset period.

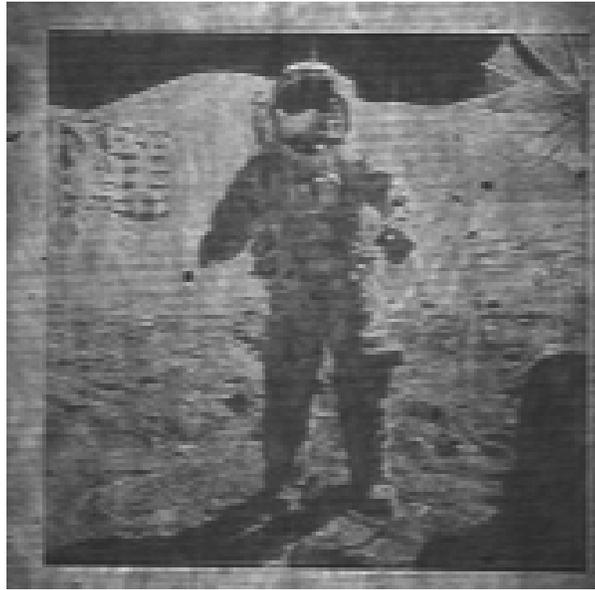


Figure 8. An image from the high-voltage 256x256 SLM operating at 1085 fps with data and high frequency coverglass pulses being applied concurrently.

#### 4. SUB-MILLISECOND PHASE-ONLY SLM SYSTEMS

The system for driving a 256 x 256 dual-frequency spatial light modulator (SLM) is shown in Figure 9. The complete system includes a dual-frequency 256x256 spatial light modulator, PCI-compatible drive electronics, high-voltage SLM interface electronics, temperature controller, 256 x 256 fast-framing Dalsa camera, camera-to-SLM interface electronics, Windows-based control software and the associated cables.

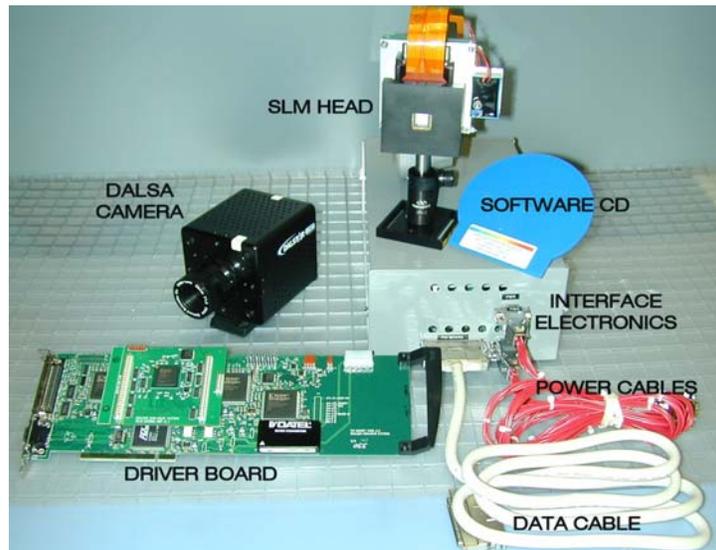


Figure 9. High-voltage 256 x 256 LCoS SLM system for driving dual-frequency nematic modulators.

## 5. CONCLUSION

The first demonstration of a high-resolution, phase-only LCoS SLM capable of providing a full wave of stroke at 670 nm with a sub-millisecond response time is reported. The system uses a high-voltage backplane with good optical quality, dual-frequency nematic liquid crystal and a proprietary drive scheme to achieve fast modulation with high optical throughput.

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