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Development of large-array spatial light modulators

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ABSTRACT

Newer silicon foundry processes make possible high-resolution backplanes (i.e. larger arrays with more line pairs per millimeter). Higher resolution is a benefit of the small geometry processes being developed for the electronics industry. Unfortunately, the trend is to shrink the circuits and decrease the operating voltage of the chip. For liquid crystal on silicon (LCoS) devices, the loss in voltage has a negative impact on performance. Higher voltage provides the excitation to achieve good response time with sufficient modulation depth from liquid crystal electro-optic modulators. This paper discusses the development of large array devices using the smaller geometry processes and some of the techniques used to retain good performance from the liquid crystal modulators.

Keywords: Liquid crystal on silicon, spatial light modulators

1. INTRODUCTION

Large array devices using Liquid Crystal on Silicon (LCoS) technology are not new. LCoS technology is being used for high definition television (HDTV)[1] along with other microdisplay technologies such as Thin Film Transisitor (TFT) and Digital Mirror Devices (DMD). Microdisplays are sometimes used as spatial light modulators (SLMs) as an alternative to devices specifically designed for SLM applications. There are several problems with using microdisplays for SLM applications such as:

- the cumbersome format (4/3 or 16/9 aspect ratios instead of 2^n square arrays),
- meager unit-circle coverage[2,3,4] ($xe^{-jk\pi(x)}$ instead of $xe^{-j2\pi(y)}$ where k is a constant having a value between 0 and 1 and x and y are independent variables ranging from 0 to 1),
- insufficient frame rate for anything other than binary operation (typically full gray scale is generated at video rates), and
- moderate spatial resolution (pixel pitch >10 microns).

Of the various deficiencies, the lack of resolution (measured in line pairs per millimeter (lp/mm) or pixel pitch) has one of the largest effects on the size and weight of the optical subsystem. As an example, the focal length, which scales the Fourier transform of the input data to the spatial frequency filter in an optical correlator, increases with the square of the pixel pitch of the SLM, assuming one SLM type is used at the input and filter planes.[5] In a typical correlator design, the optical path is basically four focal lengths from input to output, which are all affected by the SLM pixel pitch. Consequently, larger pixels produce larger optical path lengths. Longer optical paths generally add to the size and weight of the optical system, even if techniques to fold or compress the path are used. Therefore, high-resolution SLMs are a definite advantage from a system standpoint.

The electrical addressing of large arrays is another aspect that differentiates SLMs from display devices. In most processing applications, it is desirable to process data at rates that exceed 50-60 Hz. Faster than video addressing is desirable even if the input is real-time feed from a CCD camera. For example, there are a variety of processing applications that require multiple filter patterns to analyze a frame of video, such as

determining the orientation of a part as it is being inserted into an assembly. In this case, a sequence of filter patterns that detect orientation can be applied per frame, if the SLMs and detectors are capable of operating at a faster rate. Essentially, faster SLMs allow more information to be extracted or more noise to be rejected regardless of the input source or filter algorithms being used.

Aside from pure optical data processing, high-resolution SLM's are also an enabling technology for holographic data storage. As the volume of data increases, the physical size of the storage medium becomes important. Holographic methods store data in a "page" format inside a crystalline or photo-polymer medium. The use of three dimensions, as opposed to the two-dimensionality of magnetic data storage devices, is the great advantage of this technology. The current storage density of these systems is 300 Gbits/square inch, and is improving rapidly as purer storage mediums become available and data redundancy is reduced.

In this paper, we discuss the development of large array SLMs that are capable of operating at over a 1000 frames per second and have more than 50 lp/mm (<10 micron pixel pitch). Today, one device with a two-dimensional pixel array exists that fits into this category, which is a 512x512 SLM (refer to Figure 1). However, other SLMs with 100 lp/mm or more are being developed, including 1024x1024 SLM. The 512x512 device was developed three years ago. It has a 7-micron pixel pitch, and the active area is 3.6 mm x 3.6 mm. The device has a flat fill factor of approximately 84%. The load period for one frame of data is 164 μs, driving eight bits per pixel. This 512x512 system uses drive electronics that receives data over the PCI bus. The 1024x1024 device now being developed takes the design one step further by shrinking the pixel pitch to 5 microns (100 lp/mm) and retaining a load period of 164 microseconds although there is four times more data per frame.

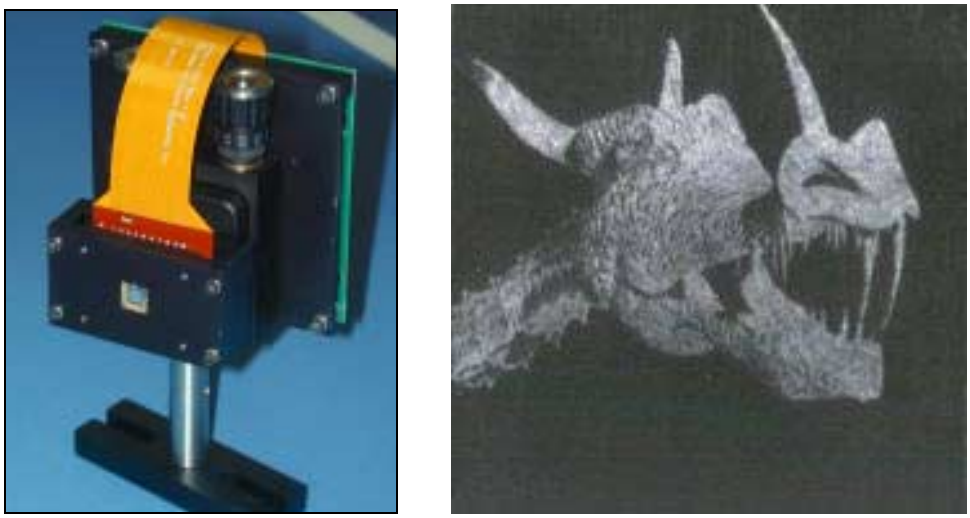

Figure 1. 512x512 (7μm) liquid-crystal-on-silicon SLM and 1 KHz gray-scale image generated by the device.

2. HIGH-RESOLUTION BACKPLANES

As the name implies, the liquid-crystal-on-silicon SLM optical head consists of a layer of liquid crystal sandwiched between a cover glass and a VLSI backplane in a PGA (pin grid array) package as shown in Figure 2. The VLSI backplane receives analog voltage signals through a limited number of input lines and routes the signals to the appropriate phase shifter element using a multiplexer arrangement (refer to Figure 3). Each array element has a storage capacitor for holding the analog voltage level on the LC addressing electrode as the other array elements are loaded or refreshed with data. Therefore, the voltage across the LC layer remains constant until new data is loaded into the array. The load rate for the whole array is faster than

the response of the LC producing a static pattern across the device. With this type of operation, data is quickly loaded into the array with a minimum number of electrical interconnects to the SLM.

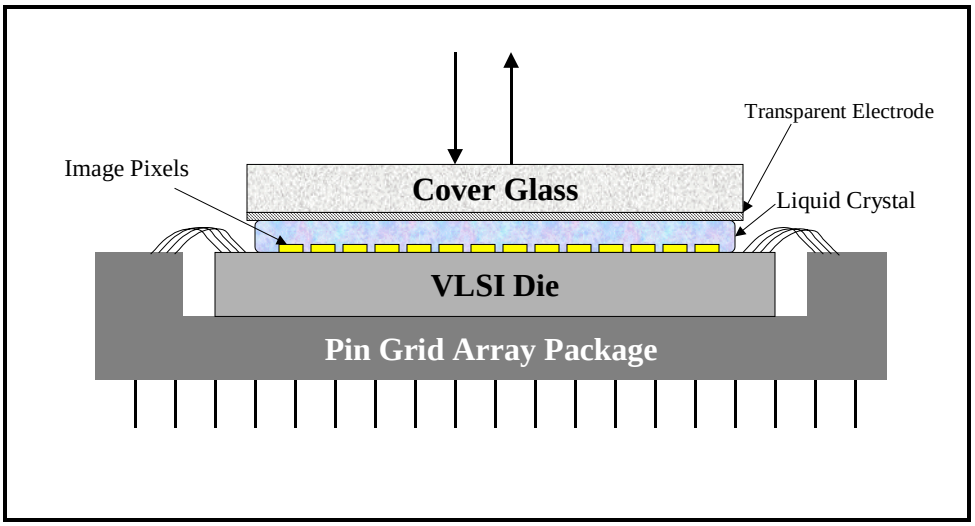

Figure 2. Drawing of an assembled SLM in cross-section.

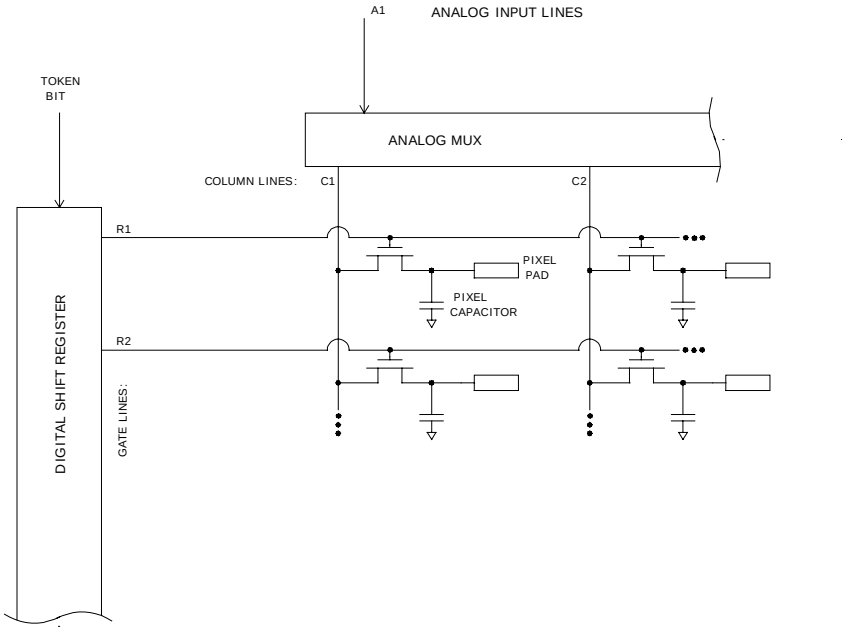

Figure 3. Block diagram of LCoS SLM addressing circuits.

The addressing structure is fabricated through commercial VLSI foundries. Most semiconductor foundries are moving to smaller geometry processes (i.e. higher resolution lithography). The smaller geometries allow greater circuit integration and provide faster circuitry with less power consumption. Today, semiconductor foundries commercially offer process sizes ranging from a few microns to a tenth of a micron. As the process size decreases, smoother (shinier) metals are used and layer thicknesses are made more uniform by

planarization techniques such as chemical-mechanical polishing (CMP). These process changes are meant to improve electrical yield, but they greatly contribute to the optical quality of the silicon backplane by eliminating topography that scatters light. Therefore, the general trend in semiconductor fabrication offers significant advantages for producing LCoS SLMs, but it is not all beneficial. Higher resolution lithography allows the electrode pitch to be reduced at the cost of reduced operating voltage.

For high-resolution backplanes, the spacing requires sub-micron foundry processes with design rules that allow the addressing circuits to be as tightly packed as the electrode structure. It is these spatial requirements that limit the operating voltage at the pixel. In the minimum one-gate-per-pixel design, shown in Figure 3, the actual drive voltage at the pixel is limited due to the body effect of the pass gates to some voltage less than the supply voltage. As the geometry of the pass gate decreases, the body effect increases which further reduces the voltage available at the pixel. Therefore, a small-geometry process may operate at supply voltages that rival larger-geometry processes, but these processes when used at their finest resolution detrimentally impact the drive capability of the device (i.e. voltage at the pixel electrode). Voltage provides the field that switches the LC modulator. The amount of voltage needed for a particular LC modulator is a function of the LC material, cell thickness and LC alignment.

With higher-resolution backplanes, the smaller pixel area reduces the capacitance at each pixel. Capacitance is needed to store charge which represents the analog data at the pixel and provides the field amplitude for controlling the LC modulator. Unfortunately, the field at the pixel is depleted as the FLC modulator switches since the polar molecules of the FLC neutralize the charge stored at the pixel. A smaller capacitance causes the field to be neutralized faster, reducing the switching capability of the pixel. To mitigate this problem, data is continuously loaded at a high data rate. The update rate is several thousand frames per second, which is achieved using high-speed drivers and parallel addressing techniques. This addressing technique for analog LCOS devices has several benefits. First, a fast update rate refreshes the charge stored at each pixel before it bleeds off. Since the field created by the charge switches the LC, a fast refresh cycle keeps the image from fading. With this capability, a strong field is maintained across the LC. A second benefit is that this technique reduces cross talk between pixels, since the active drivers are connected to a specific row and column line for a time period that is shorter than the response time of the LC. Therefore, the drive signal is confined to a single pixel, since it is the charge captured by the pixel capacitor and not the transient signal addressing the pixel that switches the LC. A third benefit is that this type of addressing scheme allows us to produce a variety of drive signals, thus giving us the capability to drive any type of LC modulator.

Figure 4 shows a floor plan and VLSI layout of the 1024x1024 chip. The addressing circuitry is at the top of the chip. This circuit multiplexes 64 analog inputs into the pixel array located in the active area. The active area is 5.12 mm (1024 x 5 μm) per side. The active area is surrounded by dummy pixels which reduce the adverse effects of chemical-mechanical polishing (CMP). CMP locally planarizes the die, removing the variations caused by the successive depositions and etching procedures used to fabricate the underlying circuitry. The planarization procedure provides tremendous improvement in the local flatness of the pixel. However, CMP is performed on the entire wafer. Between the individual die on the wafer are “scribe lines” to facilitate the cutting apart of the die on the wafer. These scribe lines produce local hills and valleys that affect the height of the polished layers. Subsequent layers conform and accentuate these irregularities. The dummy pixels provide a buffer zone from these areas to spread the dome produced by the CMP process over a larger area. With most of the curvature being at the edge of the die (outside of the active area), this configuration produces a flatter active area. Also, this dummy pixel area can be used to drive the coverglass electrode, since the dummy pixel pads are all interconnected and this connection is brought out to a bond pad. To provide the necessary bond pads for 64 data lines, control signals, power and ground connections and test signals, three sides of the chip are used. The large area between the dummy pixels and the bond pads at the top of the chip is an impedance matching circuit. Without the impedance matching circuit, the load for each data line varies, since the data signals come in on different bond pads and travel a different distance to their respective column multiplexers. For 100 MHz operation, this circuit is needed to prevent addressing artifacts at the pixels. The design is targeted for the 0.35μm silicon foundry process. The calculated fill factor

with this design is 77.4%, comparable to the fill factor of 83.6% for the 512x512 7µm pitch backplane. The actual fill factor and zero-order diffraction efficiency in the device is expected to be lower than the calculated maximum of the 5µm pitch pixel just as it was in the 7µm pitch pixel.

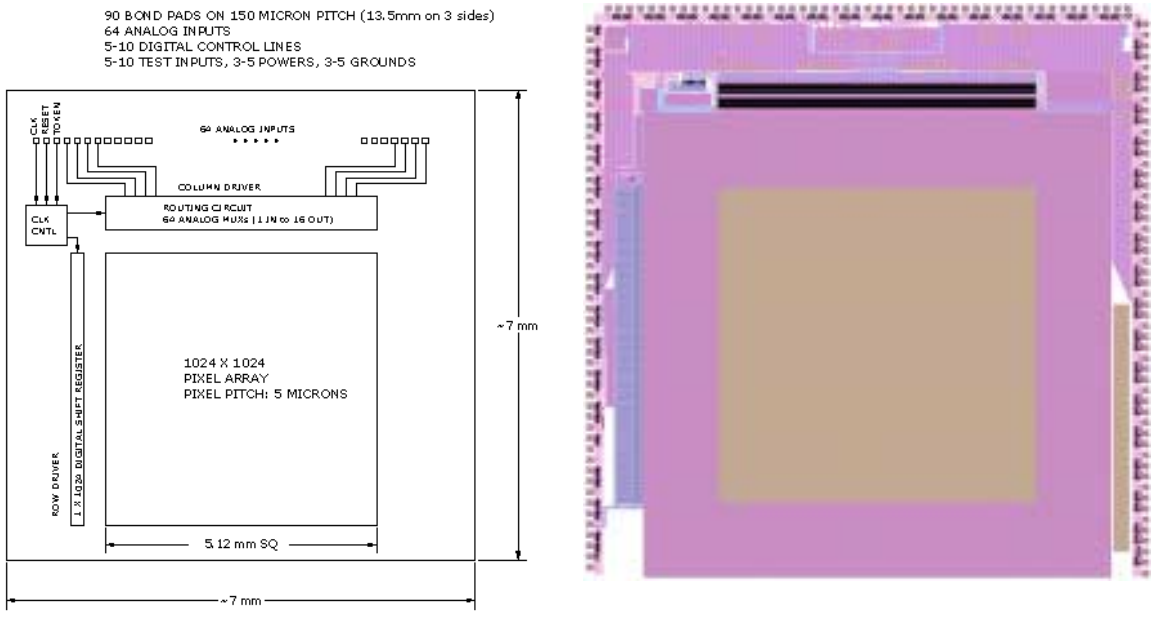

Figure 4. The floorplan and VLSI layout for a 1024x1024 chip. The active area is only 35 % of the die size, due to the dummy pixels.

3. LARGE-ARRAY SLM DRIVE ELECTRONICS

A major processing bottleneck in high-frame-rate SLM applications is the electronic interface to the SLM. This bottleneck becomes more of an issue as the array size grows. Therefore, better techniques for supplying data to the SLM need to be developed. The main goals of the next generation SLM controller include:

- Ability to drive a 1024x1024 SLM device at up to 1,000 frames per second
- Modular, extensible design
- Host-independent interfaces - e.g., a network interface, capable of a high data transfer rate
- Compatible with existing, smaller SLM products
- Small physical size
- Low power operation

With this next-generation design, there are standard communications interfaces to the core drive electronics. By removing any proprietary interface, any communications standard may be easily substituted as new ones come to market. Different possible SLM driver configurations are diagrammed in Figure 5. The communications port can follow trends in the telecommunications industry, which will make hardware for an optical 10 Gigabit Ethernet protocol more prevalent over the next two years. Likewise, DAC and analog components are being developed by the many wireless industries and will continue to improve in speed and accuracy. Of particular interest are compact DAC components operating at 100MHz and faster with 8-bit (0.4%) settling times well below 10ns.

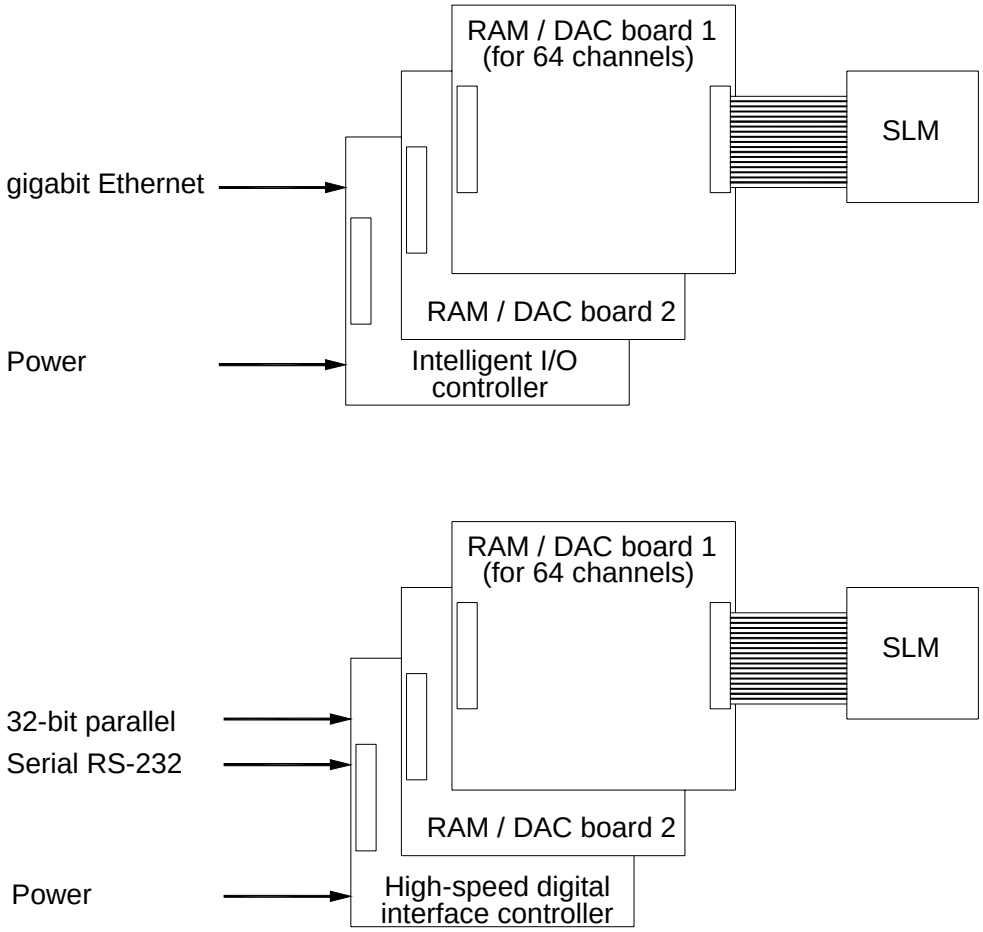

Figure 5. SLM controller system configurations.

At this time, the next-generation SLM driver hardware consists of three major modules:

- A *RAM / DAC board* provides dual-port memory that acts as a frame buffer, as well as the digital-to-analog converters (DAC's) and output amplifiers needed to drive a SLM device
- An *intelligent I/O controller*, which interfaces to a host computer or network via a gigabit Ethernet interface, and delivers data to one or two RAM / DAC boards
- A *high-speed digital interface controller*, which receives data from a digital device and loads it directly into the RAM / DAC board(s).

A SLM driver consists of either an intelligent I/O controller or a high-speed digital interface controller, married to one or two RAM / DAC boards. In addition, an external 5V DC power source is needed to provide power to the system.

RAM / DAC board

The RAM / DAC board provides the analog data interface to the SLM device. It is a modular design supporting up to 32 8-bit analog outputs. Two boards can be stacked together to accommodate up to 64 8-bit analog output channels.

Intelligent I/O controller

The intelligent I/O controller will allow a high-speed connection to a host computer, via a gigabit Ethernet network connection. The intelligent I/O controller has the following characteristics and limitations:

- Intelligent embedded system, running an embedded OS (e.g., VXworks or an embedded Linux) on a StrongARM CPU core
- Data rate from SDRAM to the RAM / DAC board(s) of approximately 239MB/S, or 239 frames per second for a 1024 x 1024 SLM, limited by IOP321's PBI bus bandwidth
- Data rate from host to SDRAM of approximately 100MB/S for the gigabit Ethernet interface
- 32 - 128 MB of local 200MHz DDR SDRAM memory, for image storage, Ethernet packet processing, and general CPU usage
- SLM timing, size, etc. configurable via software programmable registers
- Capability to synchronize SLM clock and frame to an external source, such as another controller or a camera

High-speed digital interface controller

Some applications require direct digital input, from a device like a high-speed camera or DSP board. The digital-input controller is compatible with the intelligent I/O controller, using the same form factor and RAM / DAC boards. A 32-bit or 64-bit parallel digital interface is supported. The interface consists of data lines and a clock input, which operate at up to 100MHz.

4. HIGH-SPEED, SMALL-PIXEL MODULATION

The amount of computing power versus the size and weight of the processor is a very important trade space for certain applications such as target tracking from missile and space-based platforms. Because of this, the smaller pixel pitch is an important aspect in reducing size and weight of optical subsystems. Unfortunately, the smaller pixel further restricts voltage and reduces capacitance. As discussed above, these reductions detrimentally affect FLC modulation. Therefore, BNS is testing a new modulation technique which will offset these effects. This technique uses an analog FLC modulator which allows the coverglass voltage to be flipped, doubling the effective pixel voltage.

Coverglass flipping has, in the past, not worked with analog FLC modulators for two reasons. First, FLC modulators need fields of both polarities to utilize the FLC's full modulation, speed and accuracy. With a coverglass-flipping FLC modulator, only one polarity is available to drive the molecules for any one image, and therefore the benefits of flipping the coverglass are nullified. The second problem is that coverglass-flipping schemes have historically produced a modulation gradient across the SLM. This is a result of a decrease in LC settling time for the pixels addressed immediately before the coverglass is flipped. The hardware raster scans data onto the SLM, so there is no correct time to flip the coverglass; whenever the coverglass is flipped all the rows on the SLM are in different phases of settling.

These problems are resolvable if the FLC molecules are field-treated to be pinned as a mono-domain at one extreme of their switching range. FLC consists of polar molecules that generally need both polarities to rotate through their full cone angle, and need to be driven to any given state presuming there is no physical force

pinning them to a particular state. The pinned state acts as a modulation stop and as a restoring force to return the molecules to the pinned state when no field or a negative field is applied. A positive voltage will cause the molecules to rotate in one direction through the full cone angle. Figure 6 illustrates the difference in modulation characteristics between field-treated and standard FLC modulators.

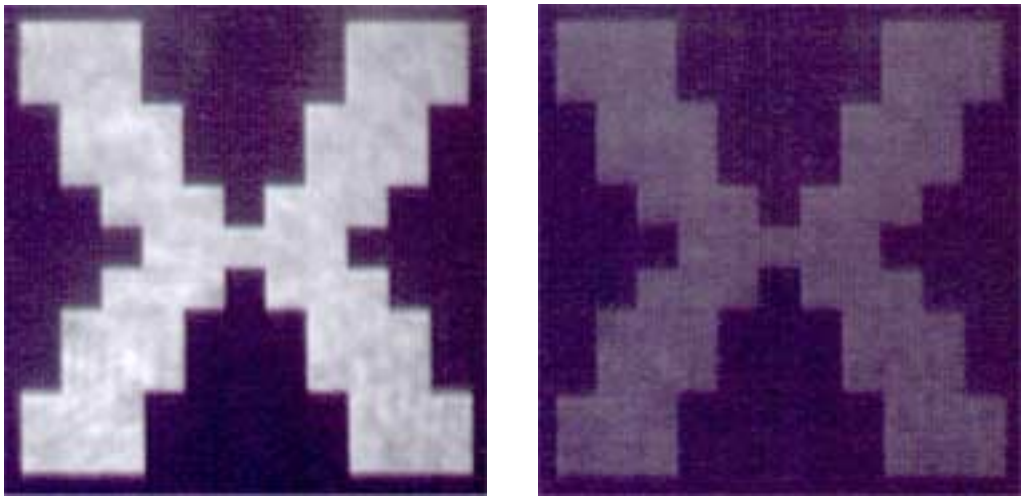

Figure 6. True (left) and inverse (right) binary images of a pinned FLC modulator.

Figure 6 demonstrates the operation of a pinned FLC modulator. The image on the left shows the LC of the large 'X' rotating 40° under an electric field of +2.5V. The background has no electric field applied. The image on the right shows the LC of the large 'X' rotating 4° in the opposite direction from the true rotation under an electric field of -2.5V. In this image it is important to note that the background still has no electric field applied to it, yet there is significantly less difference between the 'X' and background in this image than in the true image. The dissimilarity between the two images demonstrates the asymmetrical LC pinning in this device. If the LC were pinned, as it is normally, in the middle of the cone angle, the two images would appear to be exact inversions of each other. Using a field-treated FLC modulator with characteristics like those shown in Figure 7 allows for correction of both the overall modulation errors and the duty-cycle mismatches between pixels caused by flipping the coverglass. This type of modulator allows the pixel to be smaller, since less voltage and capacitance are needed for sub-millisecond operation.

5. CONCLUSION

The optical path reduction obtained by using higher resolution SLMs helps reduce the weight and size of optical systems without introducing the alignment instabilities associated with path folding and path reduction techniques. Therefore, the development of large-array devices exceeding 50 lp/mm will help advance optical processing and holographic storage systems, as long as the LC modulators and addressing electronics provide for high frame rate operation also. The developments described by this paper address these issues.

ACKNOWLEDGEMENTS

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